# Switch chips with optical ports

From Jensen Huang showcasing CPO switches at GTC 2025 to a wide range of vendors demonstrating optical engines integrated inside ASIC packages at OFC 2025, co-packaged optics ...

CPO switches shorten the electrical signal path, reduce power consumption, and decrease the number of pluggable modules by co-packaging optical modules with switch chips, while improving link reliability.

In a co-packaged design, the laser diodes, modulators and detectors are integrated on or beside the switch chip (often on a silicon photonics engine) so that the high-speed SerDes signals ...

Six optical components, each of which contains 3 1.6T silicon photonic engines, totaling 18, are placed around the switching chips. Each optical engine has 2 external laser input ports (one ...

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There are two main ways to integrate these optical engines inside the ASIC package containing the switch or XPU cores.

In data centers today, network switches in a rack of computers consist of specialized chips electrically linked to optical transceivers that plug into the system.

But the new switch uses silicon photonics to create optical interfaces in chiplet form. The chiplets are then directly attached to the switch ASIC in a package, providing major power and...

Co-packaging with optics eliminates the need for pluggable optical transceivers, lowering the overall power consumption of the switch box, reducing the congestion at the front panel, and enabling ...

Take a look inside NVIDIA silicon photonics-based networking switches that simplify manageability and design, enabling more power for compute infrastructure and delivering the scale needed to enter the ...

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